What is claimed is:

1. A ferroelectric random access memory (FRAM) device having a ferroelectric capacitor comprising:

a lower electrode formed on a semiconductor substrate;

a lower seed layer formed on the lower electrode;

a ferroelectric layer formed on the lower seed layer;

an upper seed layer formed of the same material with that of the lower seed layer on the ferroelectric layer; and

an upper electrode formed on the upper seed layer,

wherein the material for forming the upper and lower seed layers has a crystallization temperature lower than that of a material for forming the ferroelectric layer, and

the ferroelectric layer is thermally treated after the upper seed layer is formed such that the ferroelectric layer is crystallized into a stable perovskite structure and the characteristics of upper and lower interfaces of the ferroelectric layer are the same with each other.

2. The FRAM device according to claim 1, wherein the ferroelectric layer is a PZT layer.

3. The FRAM device according to claim 1, wherein the material for forming the upper and lower seed layers is a ferroelectric material having a lattice constant similar to that of a material for forming the ferroelectric layer.

4. The FRAM device according to claim 1, wherein the material for forming the upper and lower seed layers is $PbTiO_3$, TiO_3 or PZT having a more Pb content and a higher Ti/Zr ratio, than the PZT forming the ferroelectric layer.

5. The FRAM device according to claim 1, wherein the upper and lower

electrodes are formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer.

6. The FRAM device according to claim 1, further comprising a switching element and an interlayer insulating layer covering the switching element which are interposed between the semiconductor substrate and the lower electrode, and

wherein the lower electrode and a source region of the switching element are connected to each other through a contact hole formed in the interlayer insulating layer.

7. The FRAM device according to claim 1, further comprising:

a gate insulating layer between the semiconductor substrate and the lower electrode; and

source and drain regions formed on a surface of the semiconductor substrate adjacent to a periphery of the gate insulating layer.

8. A ferroelectric random access memory (FRAM) device comprising:

a semiconductor substrate;

a lower electrode formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer;

a lower seed layer formed of $PbTiO_3$, TiO_3 or PZT, on the lower electrode,

wherein the PZT having a more Pb content and a higher Ti/Zr ratio than a PZT for forming a layer to be formed on the seed layer;

a PZT layer formed on the lower seed layer;

an upper seed layer formed of the same material with that of the lower seed layer, on the PZT layer; and

an upper electrode formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer, on the upper seed layer,

wherein the material for forming the upper and lower seed layers has a

crystallization temperature lower than that of a material for forming the ferroelectric layer, and

the ferroelectric layer is thermally treated after the upper seed layer is formed such that the ferroelectric layer is crystallized into a stable perovskite structure and the characteristics of upper and lower interfaces of the ferroelectric layer are the same with each other.

9. A method for fabricating a ferroelectric random access memory (FRAM) device comprising:

forming a lower electrode on a semiconductor substrate;

forming a lower seed layer on the lower electrode;

forming a ferroelectric layer on the lower seed layer;

forming an upper seed layer on the ferroelectric layer;

thermally treating the resultant structure having the upper seed layer to make the characteristics of lower and upper faces of the ferroelectric layer be the same with each other and to complete a stable perovskite crystal structure of the ferroelectric layer; and

forming an upper electrode on the upper seed layer,

wherein the material for forming the upper and lower seed layers has a crystallization temperature lower than that of a material for forming the ferroelectric layer.

10. The method according to claim 9, the ferroelectric layer is formed of PZT.

11. The method according to claim 9, wherein the upper and lower seed layers are formed of a ferroelectric material having a lattice constant similar to that of a material for forming the ferroelectric layer.

12. The method according to claim 9, wherein the upper and lower seed layers are formed of $PbTiO_3$, TiO_2 or PZT having a more Pb content and a higher Ti/Zr

ratio than a PZT to be used to form the ferroelectric layer.

13. The method according to claim 9, wherein the lower electrode is formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer, and

the upper electrode is formed of a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer.

14. The method according to claim 9, further comprising, before the forming the lower electrode:

forming a switching element having source and drain regions on the semiconductor substrate;

forming an interlayer insulating layer on the entire surface of the semiconductor substrate having the switching element;

forming a contact hole exposing the source region through the interlayer insulating layer; and

embedding a conductive material electrically connected to the lower electrode in the contact hole.

15. The method according to claim 9, further comprising:

forming a gate insulating layer on the semiconductor substrate before the forming the lower electrode; and

forming source and drain regions on the surface of the semiconductor substrate adjacent to a periphery of the gate insulating layer by depositing impurities on the entire surface of the resultant structure having the upper electrode, after the forming the upper electrode.